IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) A display unit comprising:

a display including display elements which are combined into groups of display elements,

a circuit arrangement for controlling the display, the circuit arrangement including switches and inverters which are connected in series to form a series arrangement,

each group of the groups of display elements is connected to an output of one of the inverters, and

at least one clock bus line to supply a first clock signal and a second clock signal, wherein a first set of the switches is closed with the first clock signal when a second set of the switches is opened with the second clock signal so that after application of a third clock signal to an input of the series arrangement, at least one of the groups of display elements is

activated, wherein the display elements are arranged in N rows, and wherein a number of ~~connections to elements external to the display unit for controlling the display unit is 5 or 7~~ transistors of the groups consists of 6N transistors for non-interlaced control of the groups and 7N transistors for interlaced control of the groups.

2.(Previously Presented) The display unit as claimed in claim 1, comprising a carrier on which the display elements are arranged in a display field, wherein the at least one clock bus line extends along an edge of the display field.

3.(Previously Presented) The display unit as claimed in claim 1, wherein the groups of display elements are each formed by a row or a column of a matrix display.

4.(Previously Presented) The display unit as claimed in claim 1, wherein each switch of the switches is formed by a first n-transistor, and each inverter of the inverters is formed by a parallel arrangement of a p-transistor and a second n-transistor.

5.(Previously Presented) The display unit as claimed in claim 1, wherein the groups of display elements are connected to respective outputs of the inverters of the series arrangement.

6.(Previously Presented) The display unit as claimed in claim 5, wherein the groups of display elements include sampled rows or sampled columns of a matrix display.

7.(Withdrawn) The integrated display unit as claimed in claim 1, wherein the groups of display elements are each connected via a converter to a further clock bus line for a half-image switch-over, and converters are switched over by a signal applied to an input and/or an output of an associated inverter.

8.(Withdrawn) The integrated display unit as claimed in claim 7, wherein the converters are formed by two on/off switches each comprising a p- and an n-transistor.

9.(Withdrawn) The integrated display unit as claimed in claim 7, wherein the groups of display elements are sampled rows and/or

sampled scanning columns and/or data rows and/or data columns of a matrix display.

Claims 10-11 (Canceled)

12.(Currently Amended) A display unit comprising:

display elements;

series arrangements between the display elements, wherein each of the series arrangements includes a first switch capable of connection to a first inverter and a second switch capable of connection to a second inverter;

a first bus for a first clock for controlling the first switch;

a second bus for a second clock for controlling the second switch;

wherein the first switch and the second switch are alternately controlled by the first clock and the second clock, respectively, so that when the first switch is opened then the second switch is closed; and

a third bus for a third clock for application to an input of

one of the series arrangements so that groups of the display elements are consecutively activated, wherein the display elements are arranged in N rows, and wherein a number of ~~connections external to elements external to the display unit for controlling the display unit is 5 or 7~~ transistors of the groups consists of 6N transistors for non-interlaced control of the groups and 7N transistors for interlaced control of the groups..

Claims 13-14 (Canceled)

15.(Previously Presented) The display unit of claim 12, wherein at least one of the first bus and the second bus is arranged along an edge of the display unit.

16.(Withdrawn) A display unit comprising:

a first inverter;

a first switch connected to an input of the first inverter;

a second switch connected between an output of the first inverter and an input of a second inverter;

a first display element connectable through a third switch to

the input of the first inverter and connectable through a fourth switch to the output of the first inverter;

a second display connectable through a fifth switch to the input of the second inverter and connectable through a sixth switch to an output of the second inverter; and

clock buses for supplying a first clock to control the first switch and a second clock to control the second switch, and a third clock to one terminal of the first switch, wherein the first switch and the second switch are alternately controlled by the first clock and the second clock, respectively, so that when the first switch is opened then the second switch is closed in order to consecutively activate the first display element and the second display element.

Claim 17 (Canceled)

18.(Withdrawn) The display unit of claim 16, further comprising additional display elements that are arranged in N rows, and wherein a number of external connections for controlling the display unit is 5 or 7.

19.(Withdrawn) The display unit of claim 16, wherein at least one of the clock buses is arranged along an edge of the display unit.

20.(New) The display unit of claim 1, wherein the 6N transistors comprise 4N n-transistors and 2N p-transistors, and wherein the 7N transistors comprise 4N n-transistors and 3N p-transistors.

21.(New) The display unit of claim 1, wherein a number of connections to elements external to the display unit for controlling the display unit is 7.

22.(New) The display unit of claim 1, wherein a number of connections to elements external to the display unit for the non-interlaced control of the display unit is 5, and the number of connections is 7 for the interlaced control of the display.

23.(New) The display unit of claim 12, wherein the 6N

transistors comprise 4N n-transistors and 2N p-transistors, and wherein the 7N transistors comprise 4N n-transistors and 3N p-transistors.

24.(New) The display unit of claim 12, wherein a number of connections to elements external to the display unit for controlling the display unit is 7.

25.(New) The display unit of claim 12, wherein a number of connections to elements external to the display unit for the non-interlaced control of the display unit is 5, and the number of connections is 7 for the interlaced control of the display.